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Atty. Dkt. No. 039153-0457 (G1162)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Lopatin et al.

Title: METHOD OF USING TERNARY COPPER ALLOY TO OBTAIN A LOW RESISTANCE AND LARGE GRAIN SIZE INTERCONNECT

Appl. No.: 09/994,395

Filing Date: 11/26/2001

Examiner: Ori Nadav

Art Unit: 2811

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below.

Paul S. Hunter
(Printed Name)

(Signature)

September 23, 2005
(Date of Deposit)

AMENDMENT AND REPLY UNDER 37 CFR 1.116

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This communication is responsive to the Final Office Action dated August 25, 2005, concerning the above-referenced patent application.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this document.

Remarks/Arguments begin on page 6 of this document.

Please amend the application as follows:

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of fabricating an integrated circuit, the method comprising:

depositing an etch stop layer over a first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

depositing an insulating layer after the etch stop layer is deposited over the etch stop layer;

forming a barrier layer extending along lateral side walls and a bottom of a via aperture, the via aperture being configured to receive a via material that electrically connects the first conductive layer and a second conductive layer; and

depositing a copper alloy via material in the via aperture to form a via, the copper alloy material including Zinc (Zn) or Silver (Ag) and at least one element for increasing grain size including Calcium (Ca) or Chromium (Cr).

2. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes silver (Ag).

3. (Previously Presented) The method of claim 2, wherein the copper alloy via material includes Zinc (Zn).

4. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes one atomic percent or less of Zinc (Zn) or Silver (Ag).

5. (Cancelled)

6. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes Chromium (Cr).

7. (Previously Presented) The method of claim 1, wherein the element with a characteristic for increasing grain size is Calcium (Ca) or Chromium (Cr).

8. (Previously Presented) The method of claim 6, wherein the element with a characteristic for increasing grain size is one atomic percent or less of Chromium (Cr).

9. (Original) The method of claim 6, wherein the increased grain size is between 0.5 and 3 μm.

10. (Currently Amended) A method of using ternary copper alloy to obtain a low resistance and large grain size interconnect or via, the method comprising:

providing a first conductive layer over an integrated circuit substrate;

providing an etch stop layer over the first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

providing an insulating layer over the etch stop layer after the etch stop layer has been provided over the first conductive layer;

providing a conformal layer section extending along a bottom and sides of a via aperture positioned over the first conductive layer to form a barrier separating the via aperture from the first conductive layer;

filling the via aperture with a ternary copper alloy via material to form a ternary copper alloy via, the ternary copper alloy including at least one element for lowering resistivity and at least one of Chromium (Cr) or Calcium (Ca), wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via; and

providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer to the second conductive layer.

11. (Previously Presented) The method of claim 10, wherein the ternary copper alloy via material is at least 98 atomic percent copper.

12. (Previously Presented) The method of claim 11, wherein the ternary copper alloy via includes Zinc (Zn), Silver (Ag), or Tin (Sn).

13. (Previously Presented) The method of claim 11, wherein the ternary copper alloy via includes one atomic percent or less of Chromium (Cr) or Calcium (Ca).

14. (Cancelled)

15. (Previously Presented) The method of claim 10, wherein the element with a characteristic for increasing grain size is Calcium (Ca) or Chromium (Cr).

16. (Previously Presented) The method of claim 10, wherein the element with a characteristic for increasing grain size is one atomic percent or less of the ternary copper alloy via material.

17. (Currently Amended) A method of forming a via in an integrated circuit, the method comprising:

depositing a first conductive layer;

depositing an etch stop layer over the first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

depositing an insulating layer over the etch stop layer;

forming an aperture in the insulating layer and the etch stop layer;

providing a barrier material extending along a bottom and sides of the aperture to form a barrier layer;

filling the aperture with a ternary copper alloy via material to form a ternary copper alloy via including at least one of the following pairs of elements: Tin and Calcium; Tin and Chromium; Zinc and Chromium; Zinc and Calcium; Silver and Chromium; and Silver and Calcium, wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via; and

providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer and the second conductive layer.

18. (Previously Presented) The method of claim 17, wherein the ternary copper alloy via material includes copper (Cu), tin (Sn), and Calcium (Ca).

19. (Original) The method of claim 17, wherein the ternary copper alloy via material includes copper (Cu), zinc (Zn), and chromium (Cr).

20. (Previously Presented) The method of claim 17, wherein the ternary copper alloy is CuAgCr, or CuSnCa.

21. (Cancelled)

22. (Previously Presented) The method of claim 17, wherein the ternary copper alloy via includes stuffed grain boundaries.

23. (Original) The method of claim 17, wherein the grain size of the ternary copper alloy via is 0.5 to 3 μm.

REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 1, 10, and 17 are currently being amended.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1-4, 6-13, 15-20, 22, and 23 are now pending in this application.

Withdrawal of Finality of Rejection

In light of the previous Examiner's mistake in the previous Office Action (referring to layer 104 in U.S. Patent No. 6,399,496 B1 (Edelstein et al.) instead of layer 108) and that the new rationale for rejection made by the current Examiner was not necessitated by Applicant's amendment, Applicants respectfully request withdrawal of the finality of the rejection. See MPEP 706.07(a).

Rejections Under 35 U.S.C. § 103

Claims 1-3, 6-8, 10, 13, 15 and 16-20

On page 2 of the Office Action, Claims 1-3, 6-8, 10, 13, 15 and 16-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,159,845 (Yew et al.), in view of U.S. Patent No. 6,399,496 B1 (Edelstein et al.) and U.S. Patent No. 6,749,699 B2 (Bogel et al.). Applicants respectfully traverse the rejection.

In the Office Action on page 5, the Examiner states with respect to Applicants' Arguments:

> Applicant argues that Yew et al. do not teach depositing an insulating layer after the etch stop layer is deposited over the etch stop layer, because the examiner indicated that the insulating layer is layer 104 and the etch stop layer is layer 106, and layer 104 is not formed over layer 106.
>
> It appears that the previous examiner made a typographical error since the insulating layer should be indicated as layer 108. Layer 108 is formed over layer 106, and thus Yet et al. teach depositing an insulating layer 108 after the etch stop layer 106 is deposited over the etch stop layer, as claimed.
>
> Note that the broad recitation of the claim does not require the etch stop layer to be in direct contact with the first conductive layer.

However, Yew et al. does not disclose, suggest, or teach depositing an etch stop layer in direct contact with the first conductive layer. The Figures and the text of Yew et al. clearly show that etch stop layer 106 is not directly in contact with a conductive layer. This feature is required in all the pending claims.

In addition to Yew et al., neither Edelstein et al. nor Bogel et al. disclose, suggest, or teach "depositing an etch stop layer over a first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer." Thus, the combination of Yew et al., Edelstein et al., and Bogel et al. do not disclose or suggest all the limitations of Claims 1-3, 6-8, 10, 13, 15, and 16-20. Accordingly, the rejection cannot be properly maintained. Applicants respectfully request withdrawal of the rejection.

Claims 4 and 22

On page 3 of the Office Action, Claims 4 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al., in view of Edelstein et al. and Bogel et al., and further in view of U.S. Patent No. 6,440,849 B1 (Merchant et al.). On page 4 of the Office Action, Claims

9 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al., in view of Edelstein et al. and Bogel et al., and further in view of U.S. Patent No. 6,380,083 B1 (Gross). Applicants respectfully traverse these rejections. Claims 4 and 9 depend from Claim 1 and are patentable for at least the same reasons as Claim 1. Claims 22 and 23 depend from Claim 17 and are patentable for at least the same reasons as Claim 17. Applicants request withdrawal of the rejections.

Claims 11 and 12

On page 4 of the Office Action, Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al., in view of Edelstein et al. and Bogel et al., and further in view of U.S. Patent No. 6,090,710 (Andricacos et al.). Applicants respectfully traverse the rejection. Claims 11 and 12 depend from Claim 10 and are patentable for at least the same reasons as Claim 10. Applicants request withdrawal of the rejection.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 50-2350. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 50-2350. If any extensions of time are needed for timely acceptance of papers

submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 50-2350.

Respectfully submitted,

Date September 23, 2005

By _____

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RCE
JFW

Atty. Dkt. No. 039153-0457 (G1162)

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Appl. No.:	09/994,395
Appl. Filing Date:	11/26/2001
Examiner:	Ori Nadav
Art Unit:	2811

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**, on the date below.

PAUL S. HUNTER
(Raul S. Hunter)

(Signature)

November 10, 2005
(Date of Deposit)

CORRECTED REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This document includes a correction to the date of the previously filed Amendment to be entered and considered in the Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 filed November 2, 2005 for the above-identified application.

The RCE filed November 2, 2005 and the enclosed items listed below were filed prior to the earliest of: (1) payment of the issue fee (unless a petition under 37 C.F.R. § 1.313 is granted); (2) abandonment of the application; or (3) the filing of a notice of appeal to the U.S. Court of Appeals for the Federal Circuit under 35 U.S.C. §141, or the commencement of a civil action under 35 U.S.C. §145 or §146 (unless the appeal or civil action is terminated).

1. Submission **required** under 37 C.F.R. §1.114: (check items that apply)

a. Previously submitted:

[**X**] Please enter and consider the amendment and/or reply previously filed on **09/23/2005**. (copy of which is enclosed)

[ ] Please consider the Affidavit(s)/Declaration(s) previously filed on __ but not considered.

[ ] Please consider the arguments in the Appeal Brief or Reply previously filed on __.

[ ] Other __.

b. Enclosed are:

[ ] Amendment/Reply.

[ ] Affidavit(s)/Declaration(s).

[ ] Information Disclosure Statement.

[ ] Form PTO-1449 with copies of ___ listed reference(s).

[ ] Other .

Miscellaneous:

[ ] Suspension of action of the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of __ months.

[ ] Applicant hereby petitions for an extension of time under 37 C.F.R. §1.136(a) for the total number of months checked below:

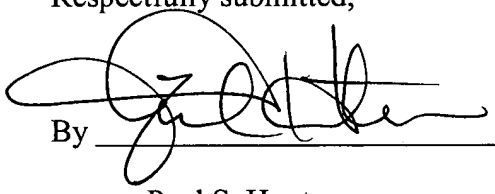
[ ] A check in the amount of [00] to cover the filing fee is enclosed.

[**X**] The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any

overpayment, to Deposit Account No. 50-2350. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 50-2350.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,



Date November 10, 2005

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